

ASSP

SWITCHING REGULATOR
CONTROLLER

MB3775

LOW VOLTAGE DUAL PWM SWITCHING
REGULATOR CONTROLLER

The MB3775 is a dual pulse-width-modulation control circuit. It contains the basic circuits required for two PWM control circuits. Complete synchronization is obtained by using the same oscillator output waveform.

This IC can provide following types of output voltage: step down, step up, and inverter. Power consumption is low, thus the MB3775 is ideal for use in high-efficiency portable equipment.

- Wide supply voltage range: 3.6 V to 18 V
- Low current consumption: 1.3 mA typical
- Wide oscillation frequency range: 1 kHz to 500 kHz
- On-chip timer latch short protection circuit
- On-chip under voltage lockout protection
- On-chip reference voltage: 1.28 V
- Variable dead time provides control over total operating range.

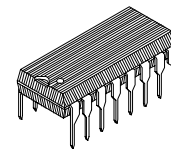
ABSOLUTE MAXIMUM RATINGS (see NOTE)

(Ta = 25°C)

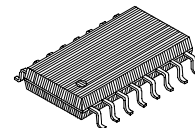
Rating	Symbol	Condition	Value	Unit
Power Supply Voltage	VCC		20	V
Error Amp. Input Voltage	Vi		-0.3 to +10	V
Collector Output Voltage	Vo		20	V
Collector Output Current	IO		75	mA
Power Dissipation	PD	Ta ≤ 25 °C(SOP)	*620	mW
		Ta ≤ 25 °C(DIP)	1000	mW
		Ta ≤ 25°C(VSOP)	*430	mW
Operating Temperature	TOP		-30 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

*: The packages are mounted on the epoxy board (4 cm x 4 cm x 1.5 mm)

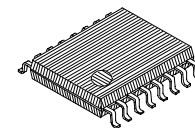
NOTE : Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



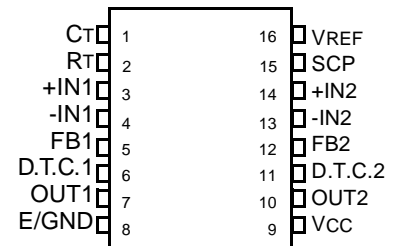
(DIP-16P-M04)



(FPT-16P-M06)



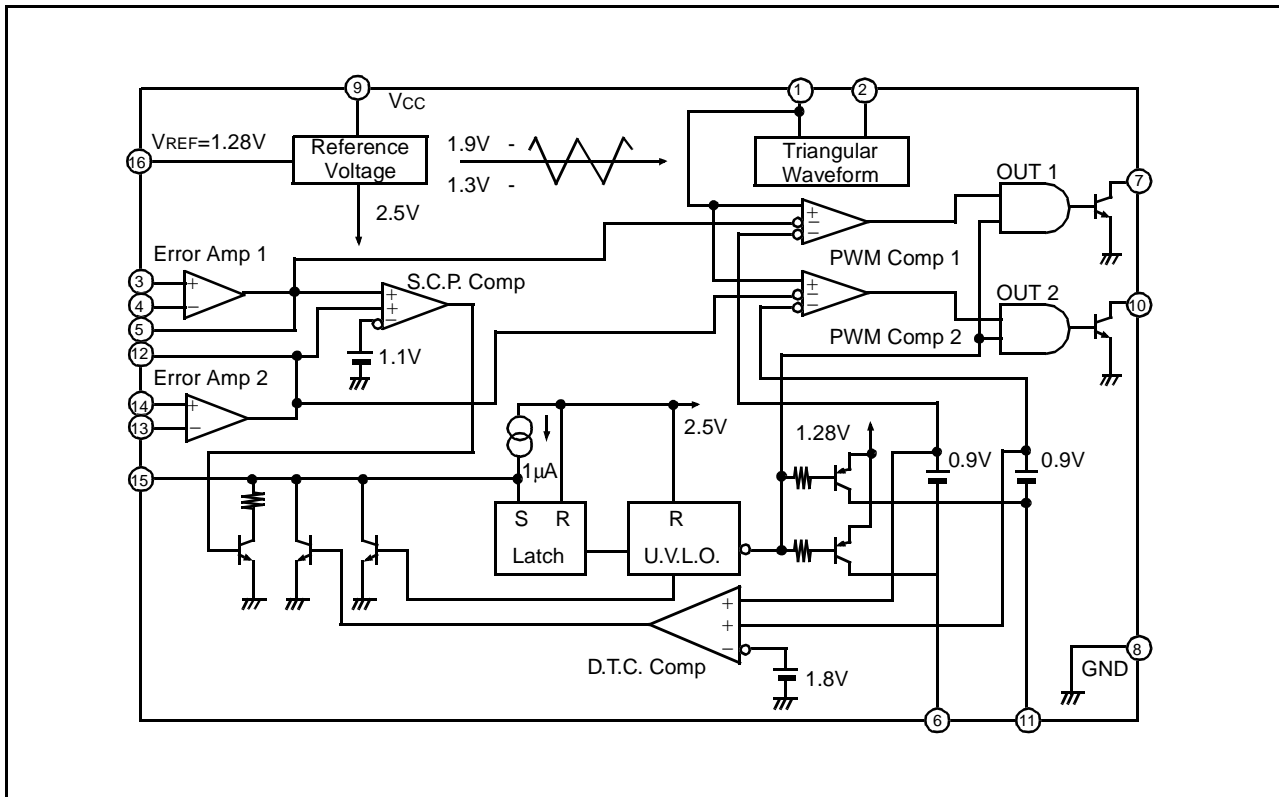
(FPT-16P-M05)

PIN ASSIGNMENT
(TOP VIEW)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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■ BLOCK DIAGRAM



■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	VCC	3.6	6.0	18	V
Error Amp. Input Voltage	VI	-0.2	-	1.45	V
Collector Output Voltage	VO	-	-	18	V
Collector Output Current	IO	0.3	-	50	mA
Phase Compensation Capacitor	CP	-	0.1	-	μF
Timing Capacitor	CT	150	-	15000	pF
Timing Resistor	RT	5.1	-	100	kΩ
Oscillator Frequency	fOSC	1	-	500	kHz
Reference Voltage Output Current	IREF	-3	-1	-	mA
Operating Temperature	TOP	-30	25	85	°C

■ OPERATION DESCRIPTION

1. Reference voltage

The reference voltage circuit generates a stable, temperature-compensated 2.5 V reference from V_{CC} (pin 9) for use by internal circuits.

A reference voltage of temperature compensated 1/2 V_{ref} can be obtained to external circuit by V_{ref} terminal (pin 16).

2. Oscillator

A triangular waveform of any frequency is obtained by connecting an external capacitor and resistor to the C_T (pin 1) and R_T terminals (pin 2).

The amplitude of this waveform is from 1.3 V to 1.9 V. The oscillator is internally connected to the non-inverting inputs of the PWM comparators. The oscillator waveform is available at the C_T terminal.

3. Error amplifiers

The error amplifier detects the output voltage of the switching regulator.

The common-mode input voltage range is -0.2 V to 1.45 V, so the input reference voltage can be set the V_{REF} and GND levels. Error amplifiers can be used as either inverting and non-inverting amplifiers.

The voltage gain is fixed. Phase compensation is possible by connecting a capacitor to the FB terminals (pins 5 and 12) of the error amplifiers.

The error amplifier output are internally connected to the inverting inputs of the PWM comparators and also to the short protection circuit.

4. Timer latch short protection circuit

The timer latch short protection circuit detects the output levels of the error amplifiers. If one or both error amplifier outputs are 1.1 V or lower, the timer circuit begins charging the externally connected protection enable capacitor.

If the output level of the error amplifier does not drop below the normal voltage range before the capacitor voltage reaches the transistor base-emitter voltage V_{BE} (\approx 0.65 V), the latch circuit turns the output drive transistor off and sets the dead time to 100 %.

5. Under voltage lockout protection circuit

An ambiguous transition state at power-on or a momentary fluctuation in the supply line may result in loss of control and may adversely affect or even destroy the system. The under voltage lockout protection circuit compares the internal reference voltage level with the supply voltage level. If the supply voltage level falls below the reference level the latch circuit is reset the output drive transistor is turned off and the dead time is set to 100 %. The protection enable terminal (pin 15) is pulled "Low".

6. PWM comparator

Each PWM comparator has two inverting inputs and one non-inverting input. This voltage-to-pulse-width converter controls the output pulse width according to the input voltage.

The PWM comparator turns the output drive transistor on when the oscillator triangular waveform is higher than the error amplifier output and the dead time control terminal voltage.

7. Output drive transistor

The open-collector output-drive transistors provide common-emitter output of 18 V dielectric capability. The output drive transistors can source up to 50 mA of drive current to the switching power transistor.

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■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, VCC=6V)

Parameter	condition	Symbol	Value			Unit
			Min	Typ	Max	

Reference Section

Output Voltage	IOR = -1 mA	VREF	1.26	1.28	1.30	V
Output Temp. Stability	Ta = -30 °C to +85 °C	VRTC	-2	±0.2	2	%
Input Stability	VCC = 3.6 V to 18 V	Line	–	2	10	mV
Load Stability	IOR = -0.1 mA to -1 mA	Load	–	1	7.5	mV
Short Circuit Output Current	VREF = 0 V	IOS	–	-30	-10	mA

Under Voltage Lockout Protection Section

Threshold Voltage	IOR = -0.1 mA	VtH	–	2.72	–	V
	IOR = -0.1 mA	VtL	–	2.60	–	V
Hysteresis Width	IOR = -0.1 mA	VHYS	80	120	–	mV
Reset Voltage (Vcc)		VR	1.5	1.9	–	V

Protection Circuit Section

Input Threshold Voltage		VtPC	0.60	0.65	0.7	V
Input Stand by Voltage	No pull up	VSTB	–	50	100	mV
Input Latch Voltage	No pull up	VI	–	50	100	mV
Input Source Current		Ibpc	-1.4	-1.0	-0.6	μA
Comparator Threshold Voltage	Pin 5, Pin 12	VtC	–	1.1	–	V

Triangular Waveform Oscillator Section

Oscillator Frequency	C _T = 330 pF, R _T = 15 kΩ	fosc	–	200	–	kHz
Frequency Deviation	C _T = 330 pF, R _T = 15 kΩ	fdev	–	10	–	%
Frequency Stability (VCC)	VCC = 3.6 V to 18 V	fdV	–	1	–	%
Frequency Stability (Ta)	Ta = -30 °C to +85 °C	fdT	-4	–	4	%

Dead-Time Control Section

Input Threshold Voltage (fosc = 10 kHz)	Duty Cycle = 0 %	Vt0	–	1.0	VREF -0.15	V
	Duty Cycle = 100 %	Vt100	0.2	0.4	–	V
Input Bias Current		Ibdt	–	-0.2	-1	μA
Latch Mode Source Current	Vdt = 0.7 V	I _{dt}	–	-150	-80	μA
Latch Input Voltage	I _{dt} = -40 μA	Vdt	VREF -0.1	–	–	V

■ ELECTRICAL CHARACTERISTICS (Continued)

(Ta=25°C, VCC=6V)

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	

Error Amp. Section

Input Offset Voltage	VO = 1.6 V	VIO	-10	–	+10	mV
Input Offset Current	VO = 1.6 V	IIO	-100	–	+100	nA
Input Bias Current	VO = 1.6 V	IB	-500	-100	–	nA
Common Mode Input Voltage Range	VCC=3.6V to 18V	VICR	-0.2	–	+1.45	V
Voltage Gain		Av	84	120	–	V/V
Frequency Band Width	Av = -3 dB	BW	–	3	–	MHz
Common Mode Rejection Ratio		CMRR	60	80	–	dB
Max. Output Voltage Width		VOM+	2.2	2.4	–	V
		VOM-	–	0.7	0.9	V
Output Sink Current	VO = 1.6 V	IOM+	24	50	–	μA
Output Source Current	VO = 1.6 V	IOM-	–	-1.2	-0.7	mA

PWM Comparator Section

Input Threshold Voltage (fosc=10 kHz)	Duty Cycle = 0 %	Vt0	–	1.9	2.1	V
	Duty Cycle = 100 %	Vt100	1.05	1.3	–	V
Input Sink Current	Pin 5, Pin 12 = 1.6 V	IIN+	24	50	–	μA
Input Source Current	Pin 5, Pin 12 = 1.6 V	IIN-	–	-1.2	-0.7	mA

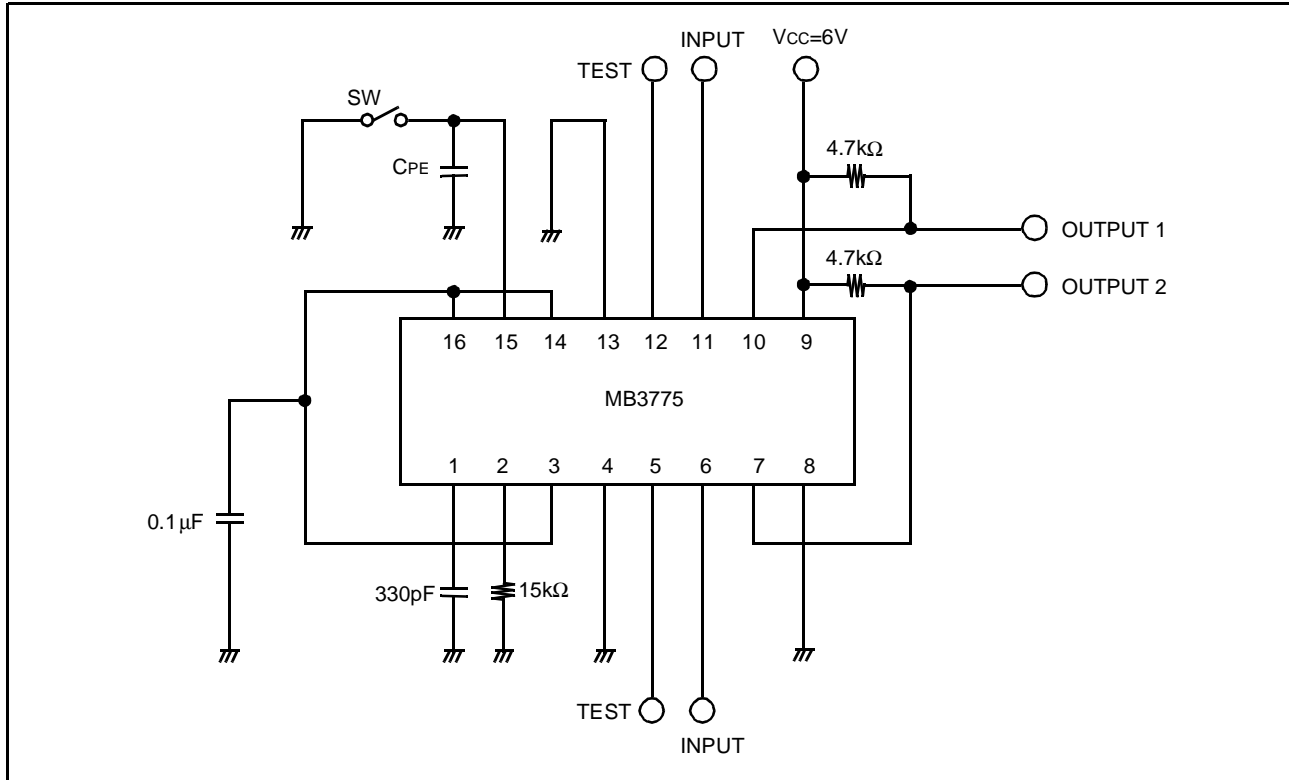
Output Section

Output Leak Current	VO=18V	Leak	–	–	10	μA
Output Saturation Voltage	IO=50 mA	VSAT	–	1.1	1.4	V

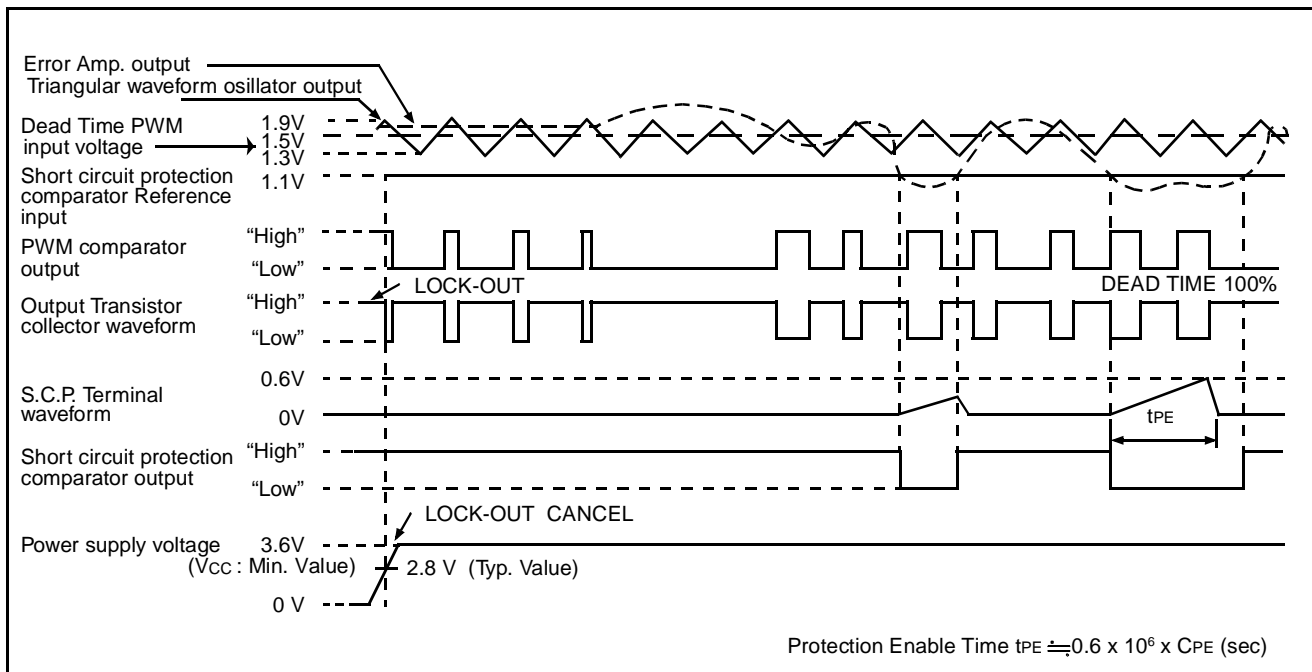
Stand by Current	Output "OFF"	ICCS	–	1.3	1.8	mA
Average Supply Current	RT=15kΩ	ICCa	–	1.7	2.4	mA

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■ TEST CIRCUIT

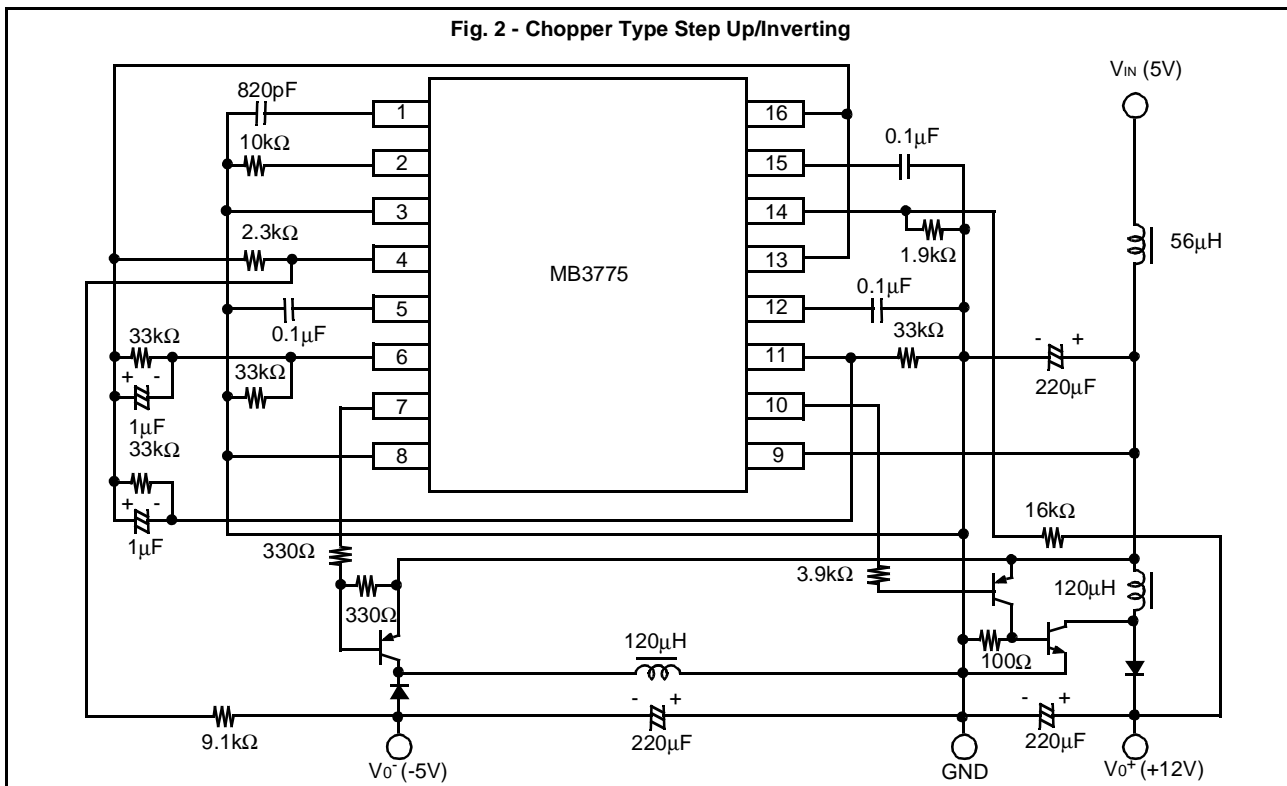
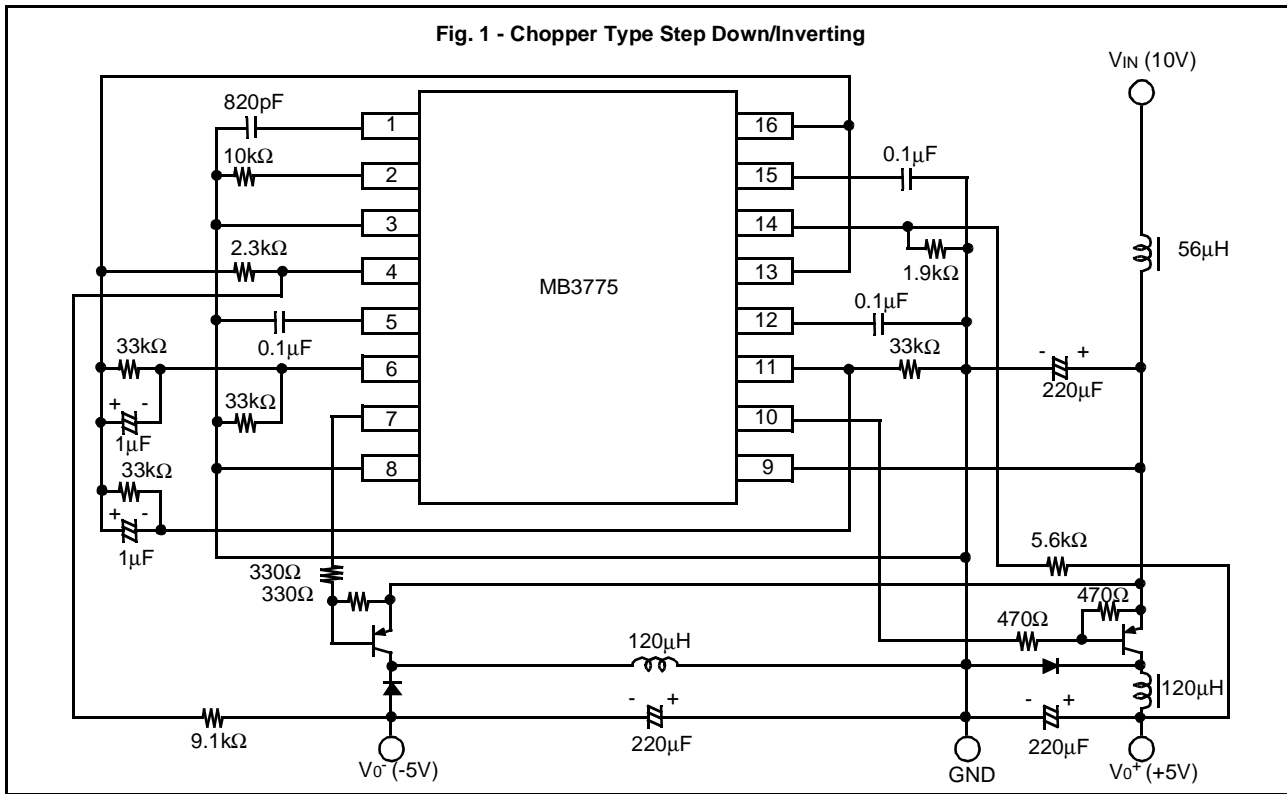


■ TIMING CHART (Internal Waveform)



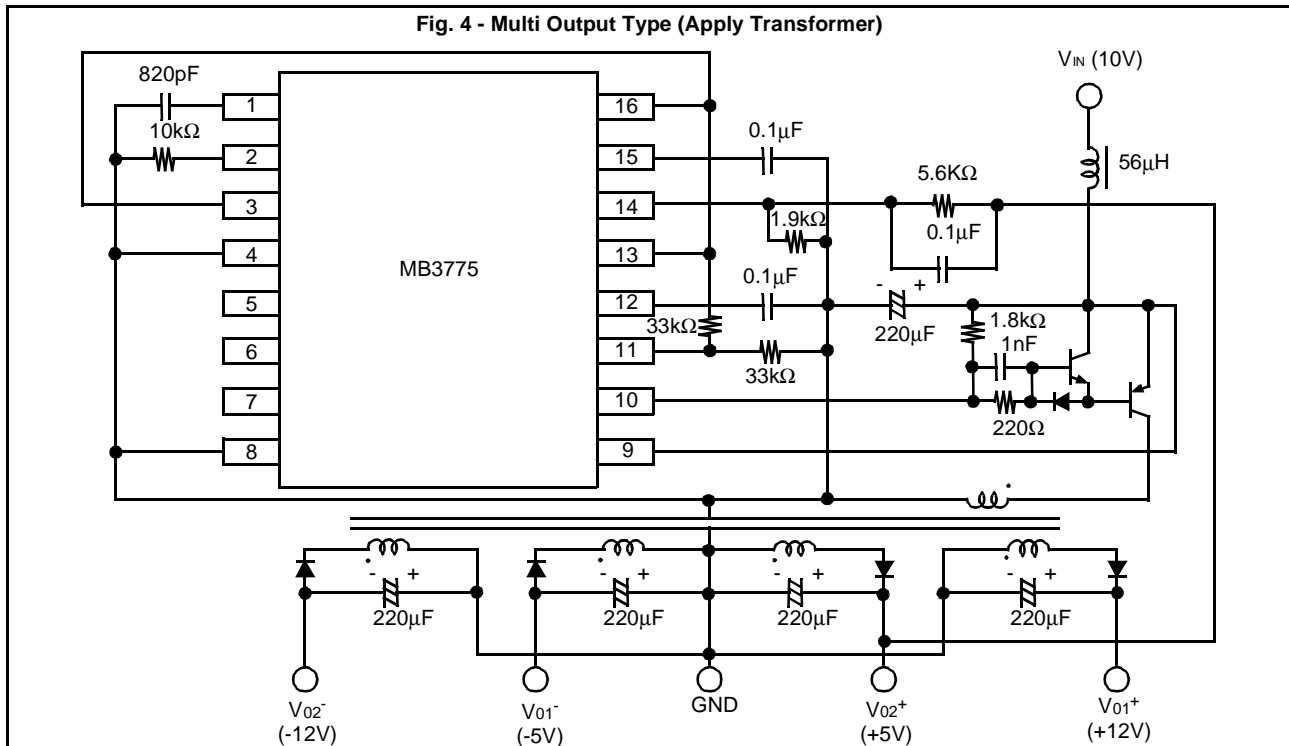
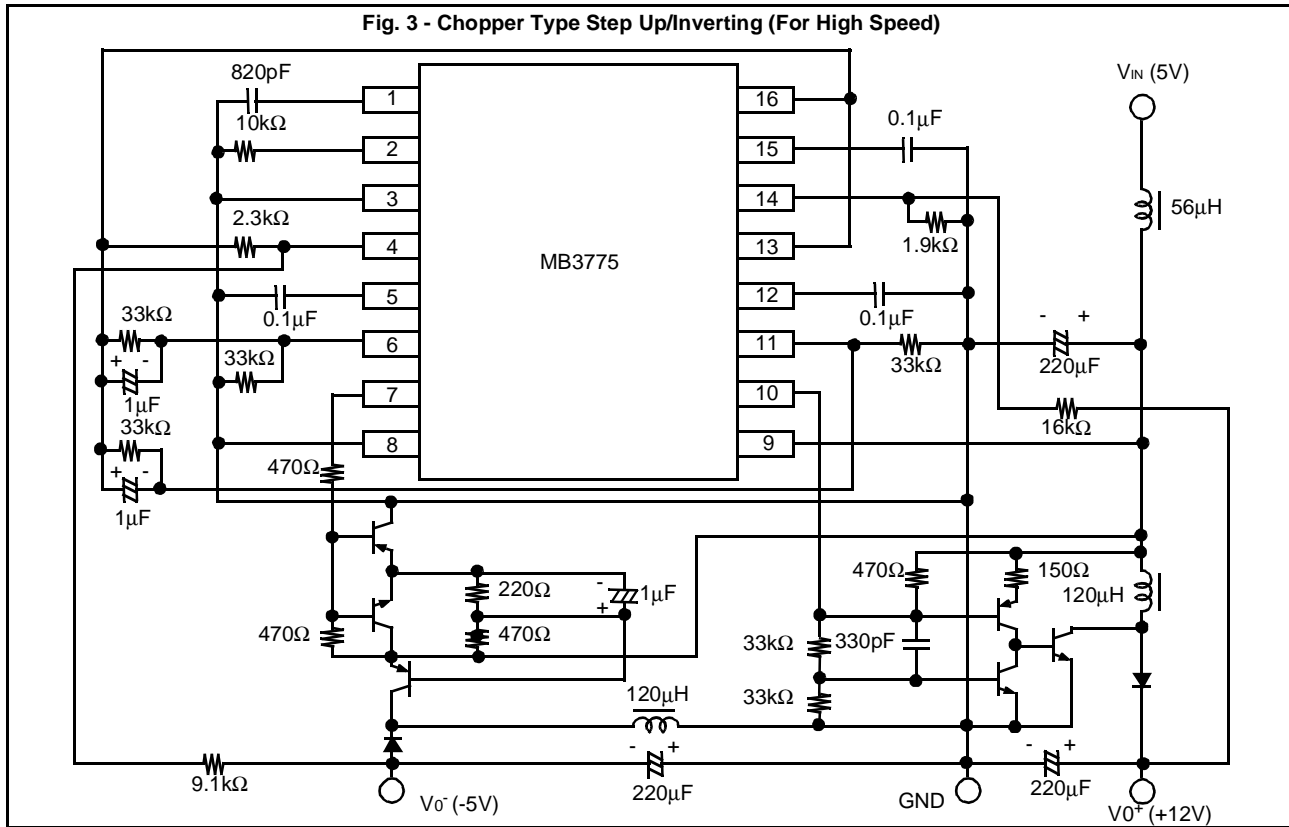
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APPLICATION CIRCUIT



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■ APPLICATION CIRCUIT (Continued)

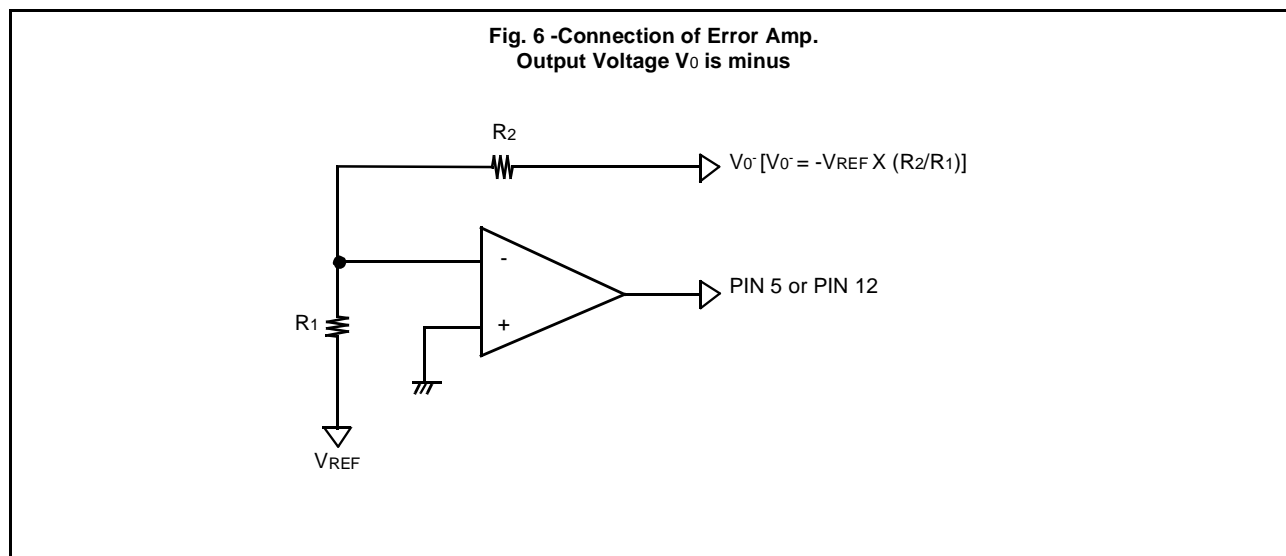
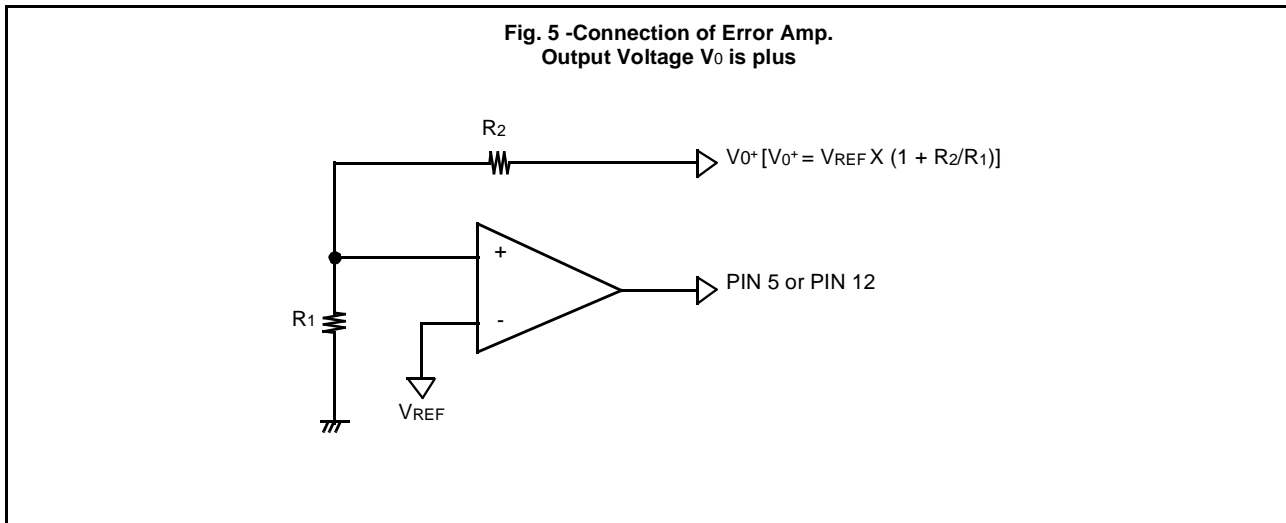


■ HOW TO SET OUTPUT VOLTAGE

The output voltage is set using the connection shown in Fig. 5 and 6.

The error amplifiers are supplied to the internal reference voltage circuit as are the other internal circuits. The common-mode input voltage range is from -0.2 V to +1.45 V.

When the amplifiers are operated non-inverting, tie the inverting terminal to V_{REF} (≈ 1.28 V). When the amplifiers are operated inverting, tie the non-inverting terminal to ground.



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■ HOW TO SET TIME CONSTANT FOR TIMER LATCH SHORT PROTECTION CIRCUIT

TIMING CHART shows the configuration of the protection latch circuit.

Error amplifier outputs, are internally connected to the non-inverting inputs of the short-circuit protection comparator and are compared with the reference voltage (1.1 V) connected to the inverting input.

When the load condition of the switching regulator is stable, the error amplifier has no output fluctuation. Thus, short-circuit protection control is also kept in balance, and the protection enable terminal (pin 15) voltage is kept at about 50 mV.

If the load condition drastically changes due to a load short-circuit and if low-level signals (1.1 V or lower) are input to the non-inverting inputs of the short-circuit protection comparator from the error amplifiers, the short-circuit protection comparator outputs a "Low" level to turn transistor Q₁ off. The protection enable terminal voltage is discharged, and then the short-circuit protection comparator charges the externally connected protection enable capacitor C_{PE} according to the following formula:

$$V_{PE} = 50 \text{ mV} + t_{PE} \times 10^{-6}/C_{PE}$$

$$0.65 = 50 \text{ mV} + t_{PE} \times 10^{-6}/C_{PE}$$

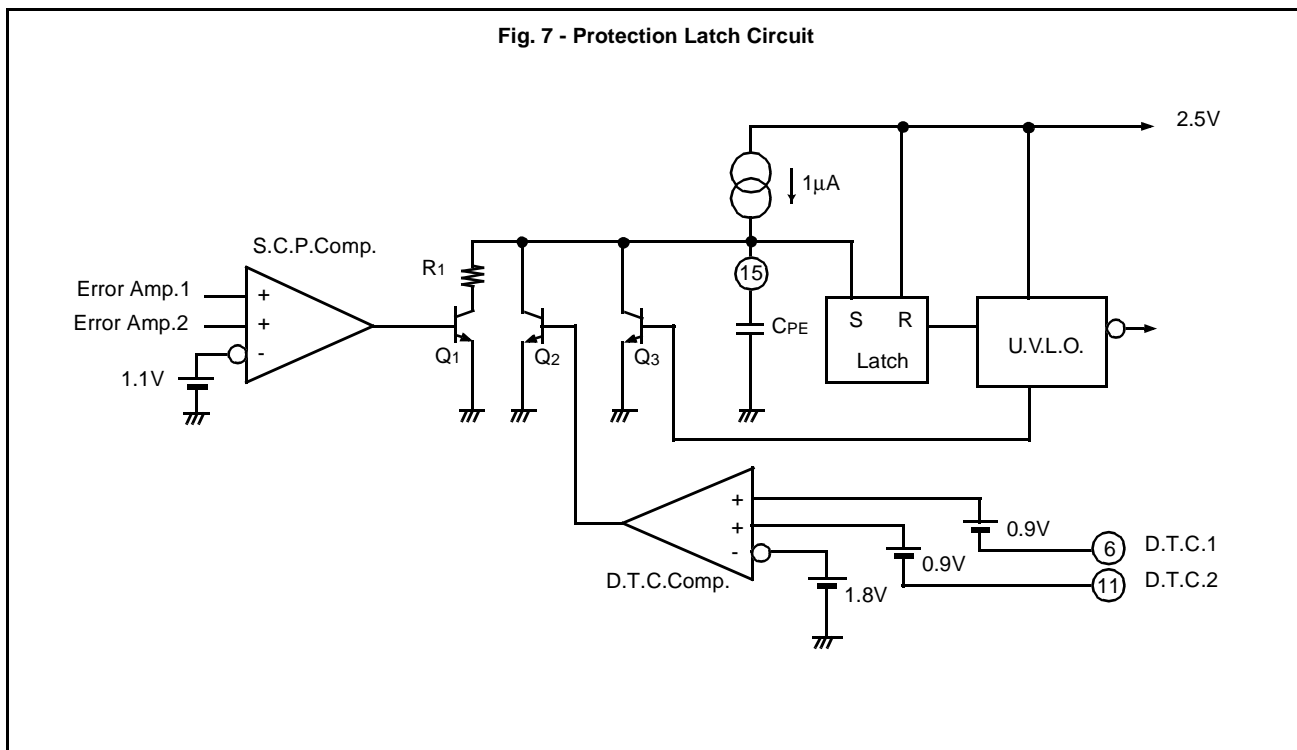
$$C_{PE} = t_{PE}/0.6 \text{ (}\mu\text{F)}$$

When the protection enable capacitor charges to about 0.65 V, the protection latch is set to enable the under voltage lockout protection circuit and to turn the output drive transistor off. The dead time is set to 100 %.

Once the under voltage lockout protection circuit is enabled, the protection enable is released; however, the protection latch is not reset if the power is not turned off.

The non-inverting inputs of the D.T.C. comparator are connected to the D.T.C. terminals (pins 6 and 11) through the power supply (about 0.9 V) and are compared with a reference voltage (about 1.8 V) connected to the inverting input.

To prevent malfunction of the short protection circuit in soft-start mode (using D.T.C. terminals), the D.T.C. comparator outputs a "High" level to turn Q₂ on until the D.T.C. terminal voltage drops to about 0.9 V.



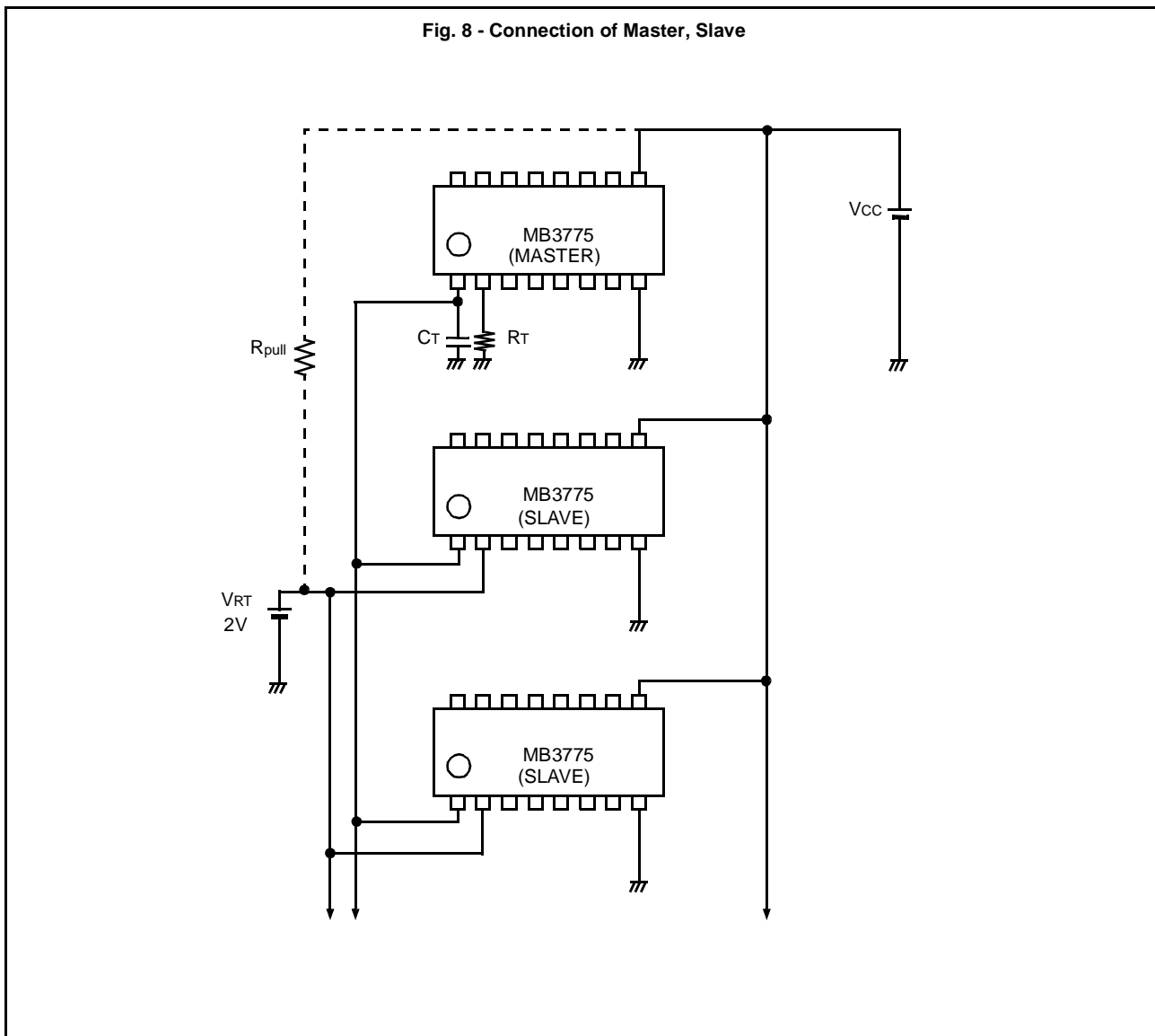
■ SYNCHRONIZATION OF ICs

To synchronize MB3775 ICs, first, the specified capacitor and resistor are connected to the C_T and R_T terminals of the master IC to start self oscillation. Next, 2 V is applied to the R_T terminals of the slave ICs to disable the charge/discharge circuit for triangular wave oscillation. Finally, the C_T terminals of the master and slave ICs are connected.

Instead of applying V_{RT} to the R_T terminals, these terminals can be pulled up by a resistor (see resistance indicated by the dashed line in Fig. 8). Select the pull-up resistance R_{pull} from the formula given below.

$$\frac{V_{CC}}{0.5 \times N} \leq R_{pull}$$

R_{pull} : Pull up Resistor (k Ω)
 V_{CC} : Power Supply Voltage (V)
 N : Number of Slave ICs



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■ TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 9 - Power supply voltage vs. Reference voltage

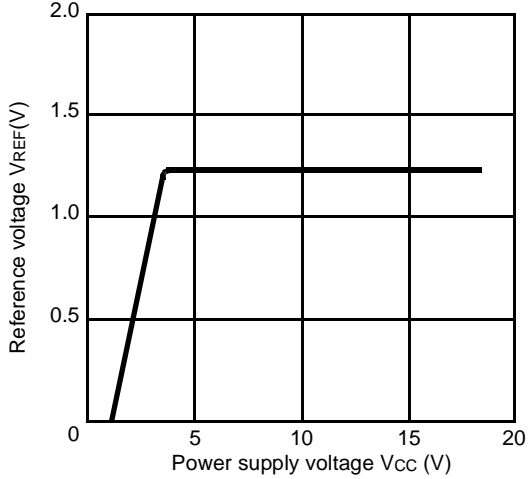


Fig. 10 - Power supply voltage vs. Average supply current

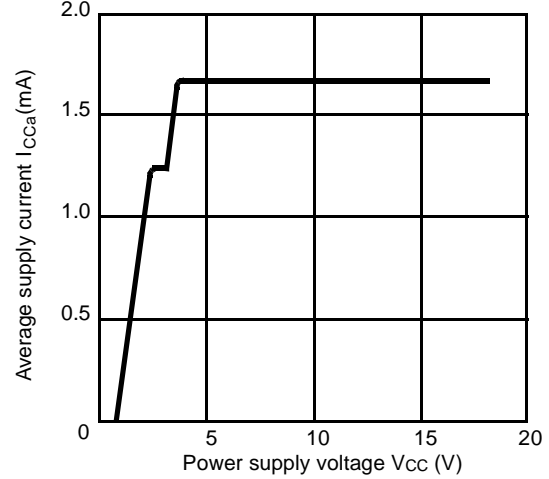


Fig. 11 - Power supply voltage vs. Stand by current

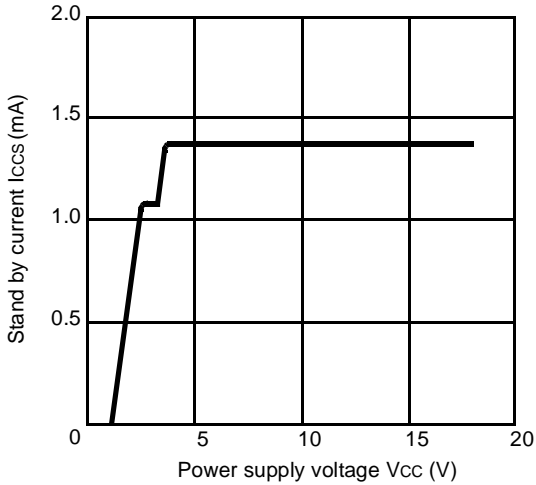


Fig. 12 - Reference voltage vs. Temp.

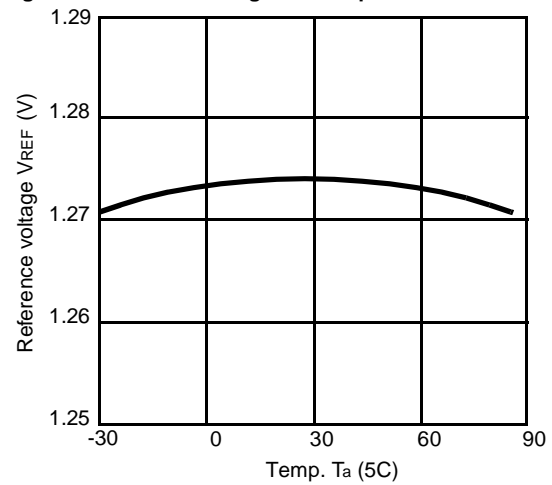


Fig. 13 - Collector saturation voltage vs. Sink current

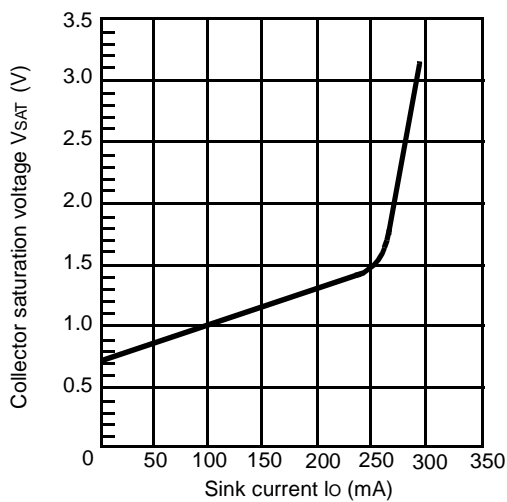
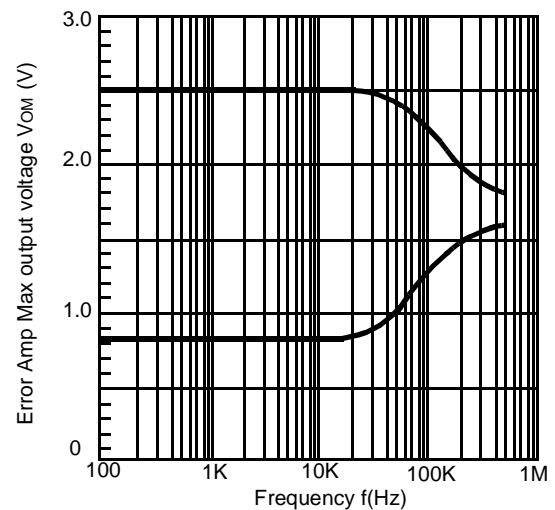


Fig. 14 - Error Amp. Max. output voltage vs. Frequency



■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig. 15 - Timing resistor vs. Oscillation Frequency

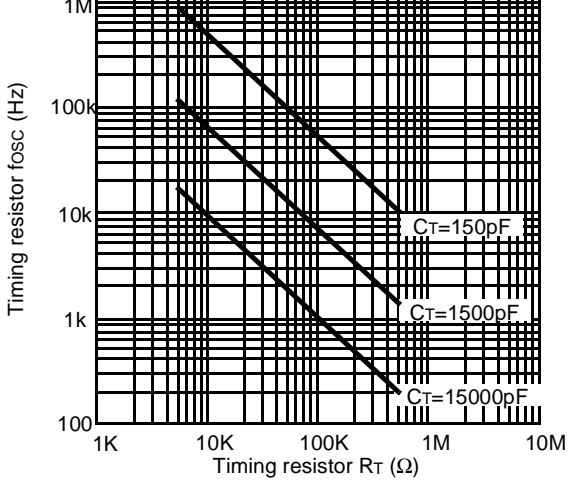


Fig. 16 - Triangular waveform cycle vs. Timing capacitor

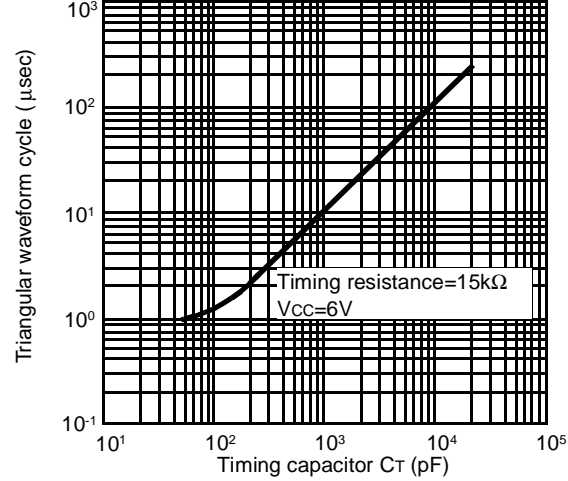


Fig. 17 - Timing capacitor vs. Triangular waveform Max. Amplitude voltage

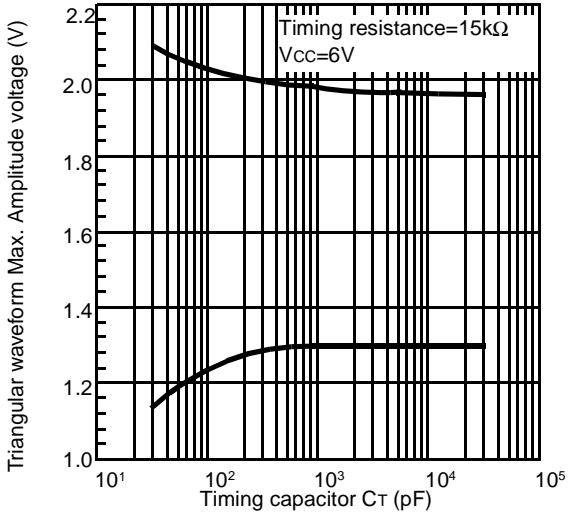


Fig. 18 - Frequency vs. Gain/Phase

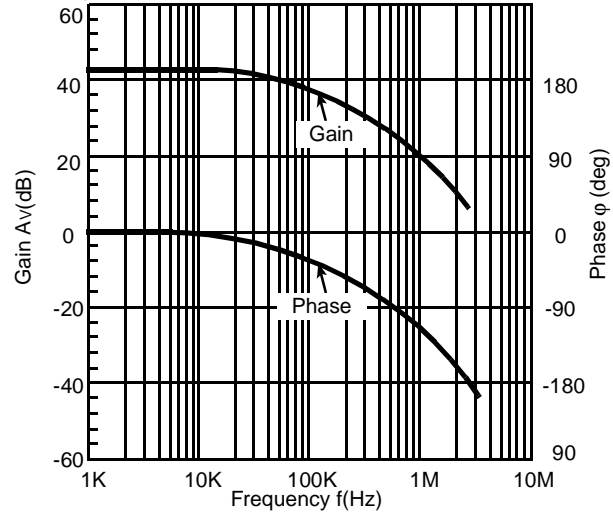


Fig. 19 - Frequency vs. Gain/Phase (Actual Data)

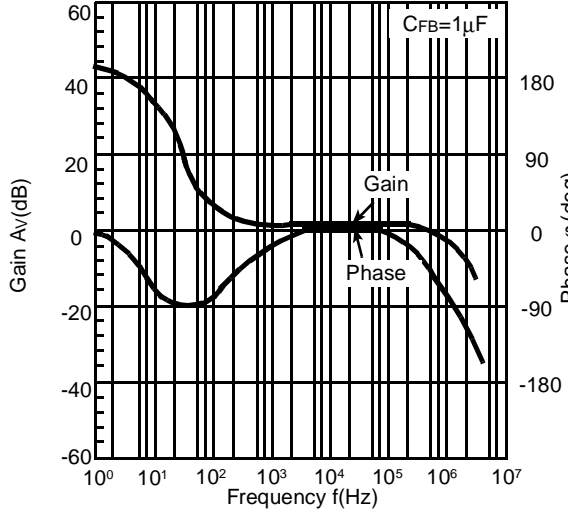
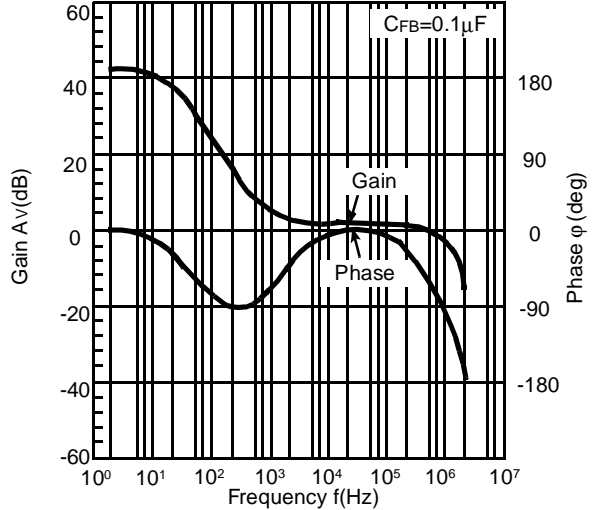
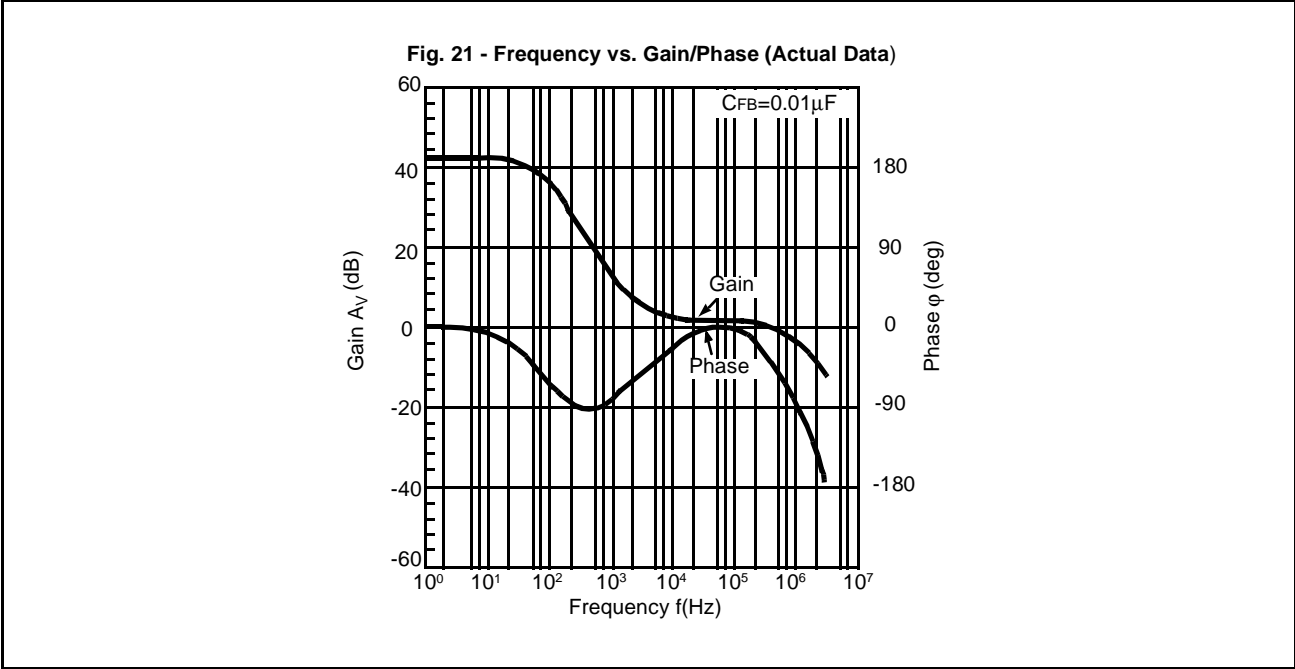


Fig. 20 - Frequency vs. Gain/Phase (Actual Data)



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■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



■ APPLICATION

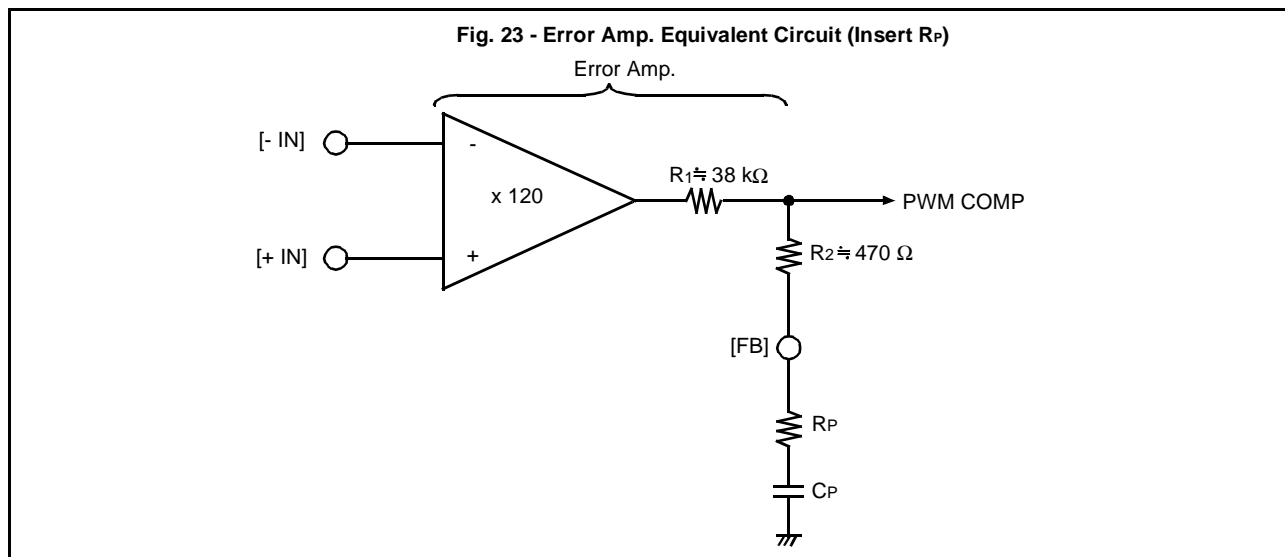
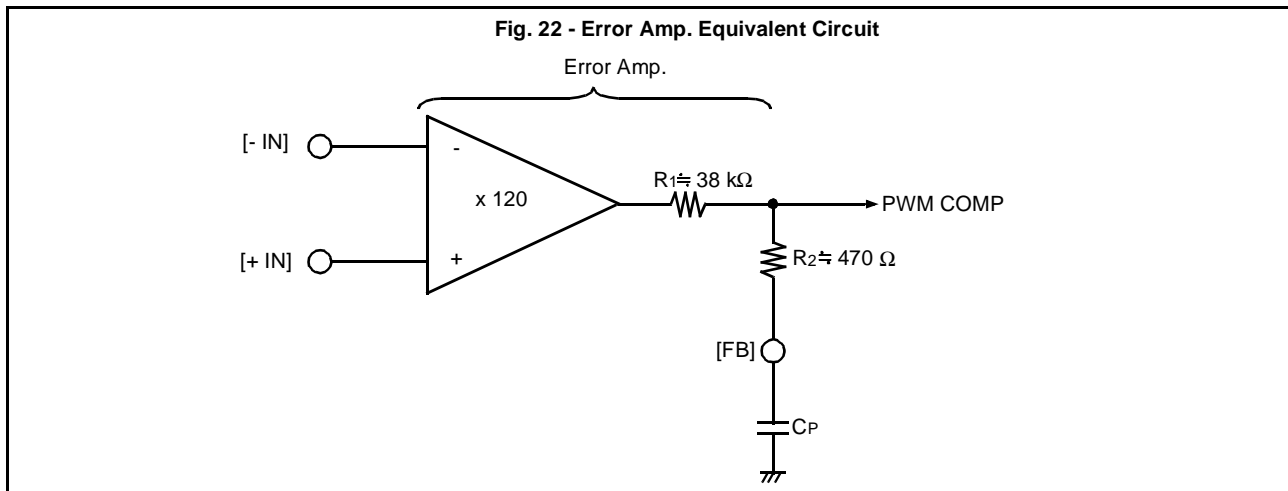
1. How to set the error amplifier frequency characteristic

Figure 22 shows the equivalent circuit of the error amplifier.

The frequency characteristic of the error amplifier is set by R_1 , R_2 , and C_P . The high-frequency gain is set by the ratio of resistors R_1 and R_2 in the IC (set value $\cong 0$ dB).

When $C_P = 0.1 \mu\text{F}$, the gain at $20 \text{ kHz} \leq f \leq 5 \text{ MHz}$ is about 0 dB. The roll-off frequency is adjusted by changing external phase compensating capacitor C_P (see Fig. 24).

When high frequency gain is needed or the phase must be advanced at a low frequency, connect a resistor R_P between the FB terminal and C_P as shown in Figure 23 (see Fig. 25).



NOTE: As shown above, the frequency characteristic of the error amplifier is set by the external phase compensating capacitor C_P .

When a ceramic chip capacitor must be used to meet the requirements of a small system, be careful of its temperature characteristic. ($-30^\circ\text{C} \cong 1/5$ and $80^\circ\text{C} \cong 1/3$ for the frequency characteristic, so a sufficient phase margin must be allowed for at room temperature.) Ceramic chip capacitors with a low temperature characteristic (B characteristic) or film capacitors are recommended (see Fig. 26 to 28).

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Fig. 24 - Error Amp. Frequency characteristics

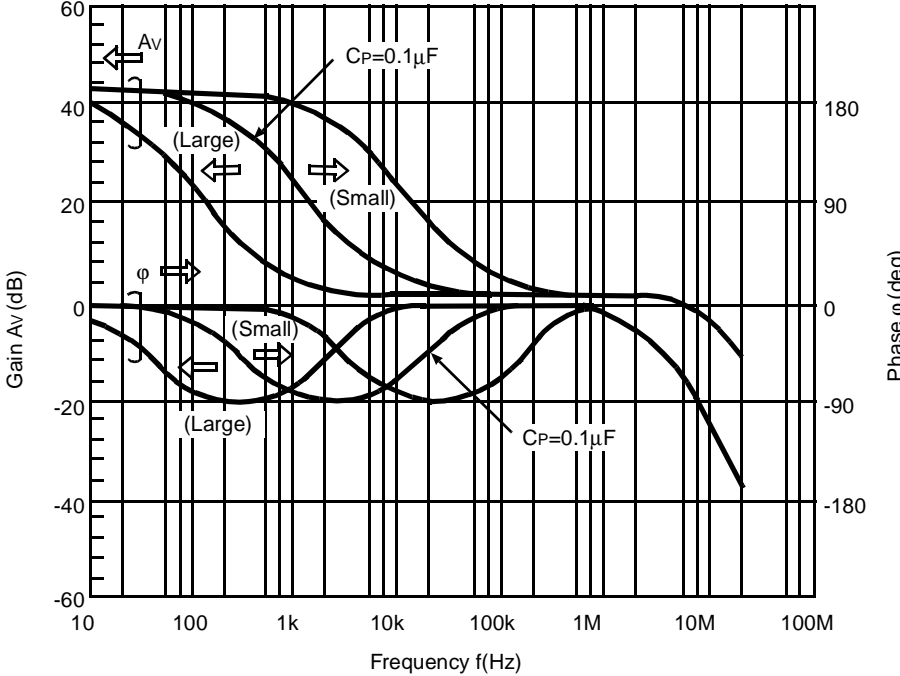


Fig. 25 - Error Amp. Frequency characteristics

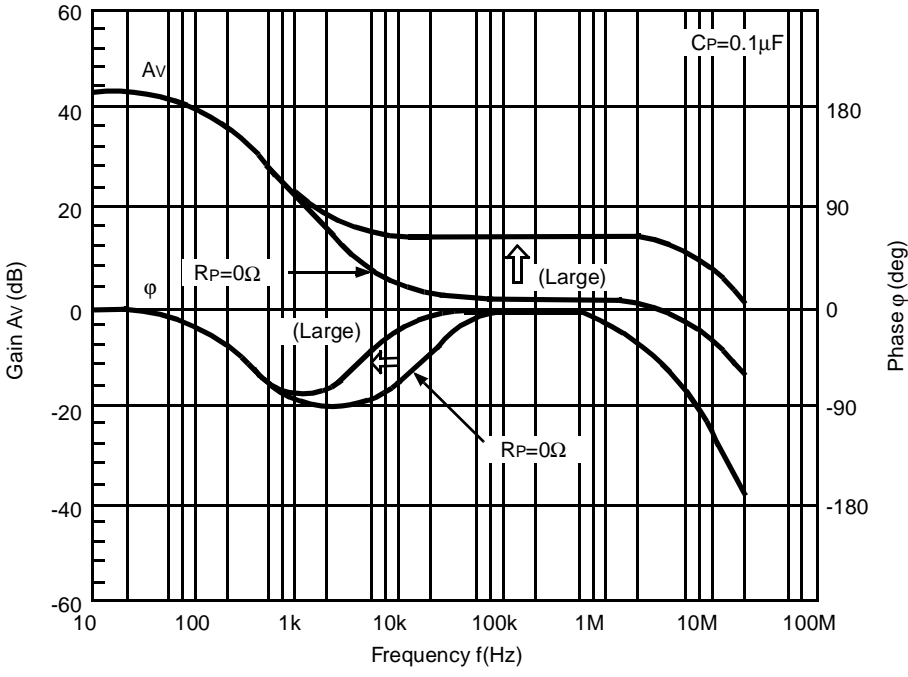


Fig. 26 - Ceramic Chip Capacitor (0.1 μ F)

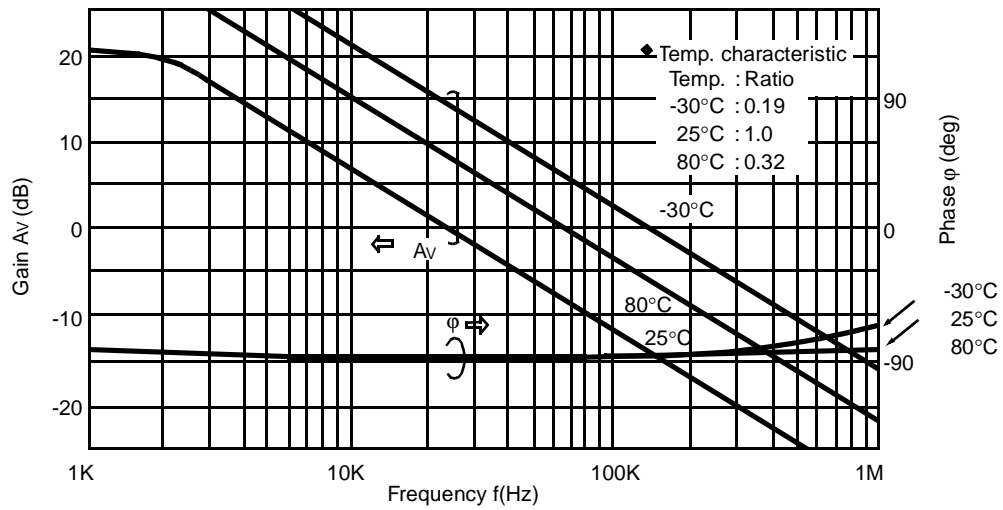


Fig. 27 - Tantal Capacitor (0.33 μ F)

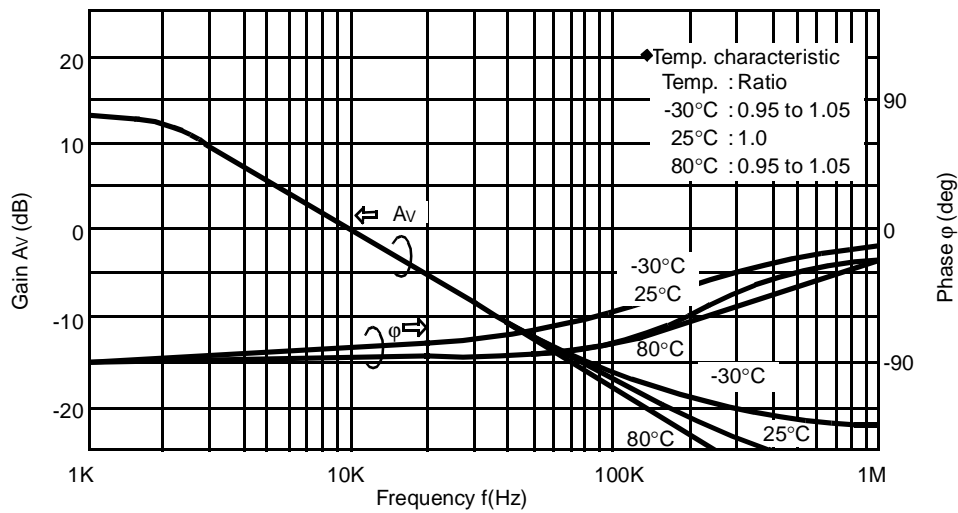
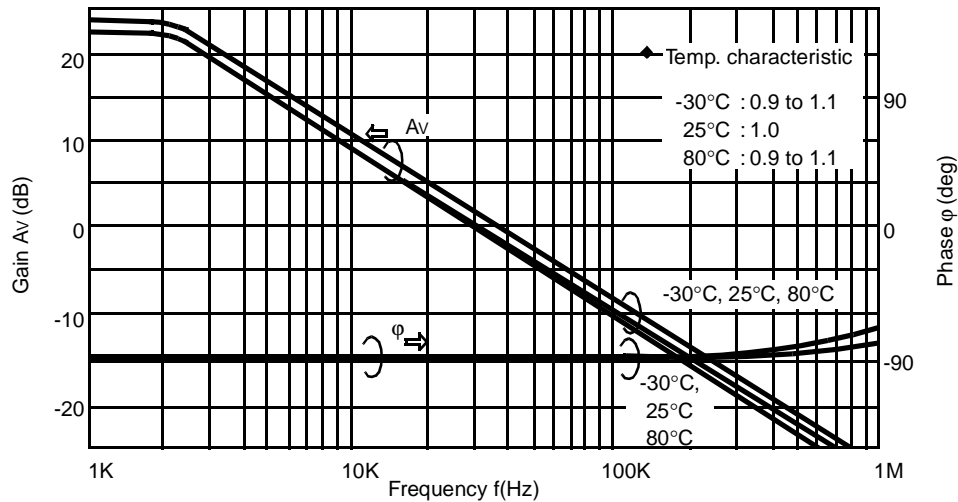


Fig. 28 - Film Capacitor (0.1 μ F)



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2. Effect of equivalent series resistance of smoothing capacitor

The equivalent series resistance (ESR) of the smoothing capacitor in the DC/DC converter greatly affects the loop phase characteristic. A smoothing capacitor with a low ESR reduces system stability by increasing the phase shift in the high-frequency region (see Fig. 30). Therefore, a smoothing capacitor with a high ESR will improve system stability. Be careful when using low ESR semiconductor electrolytic capacitors (OS-CON) and tantalum capacitors.

Fig. 29 - Step Down DC/DC Converter Basic Circuit

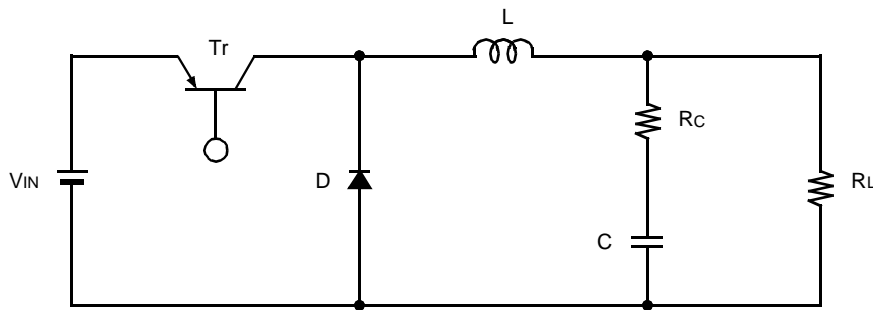


Fig. 30 - Gain vs. Frequency

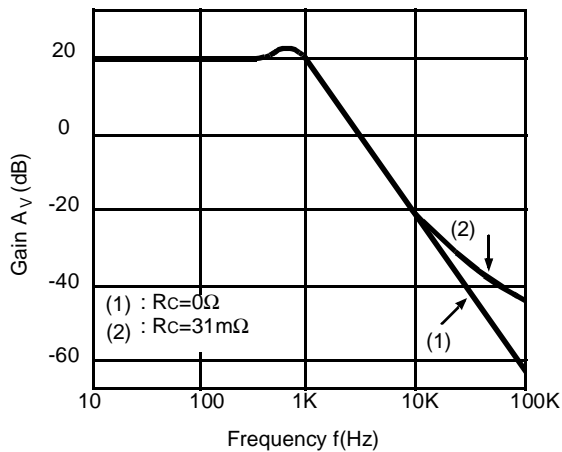
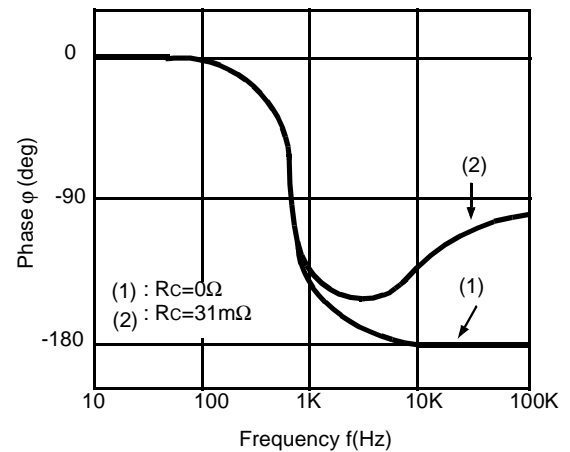
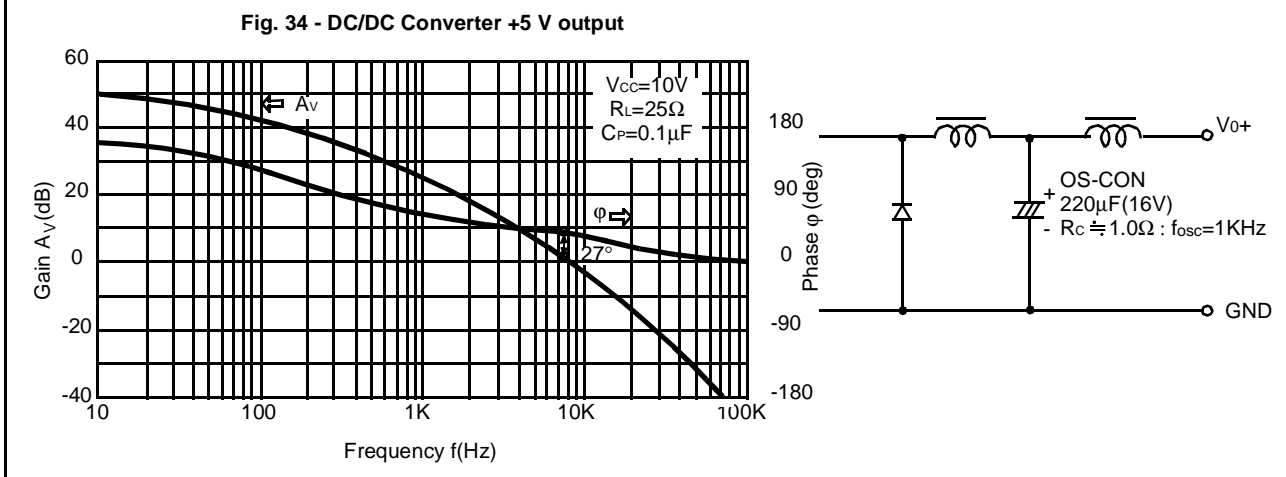
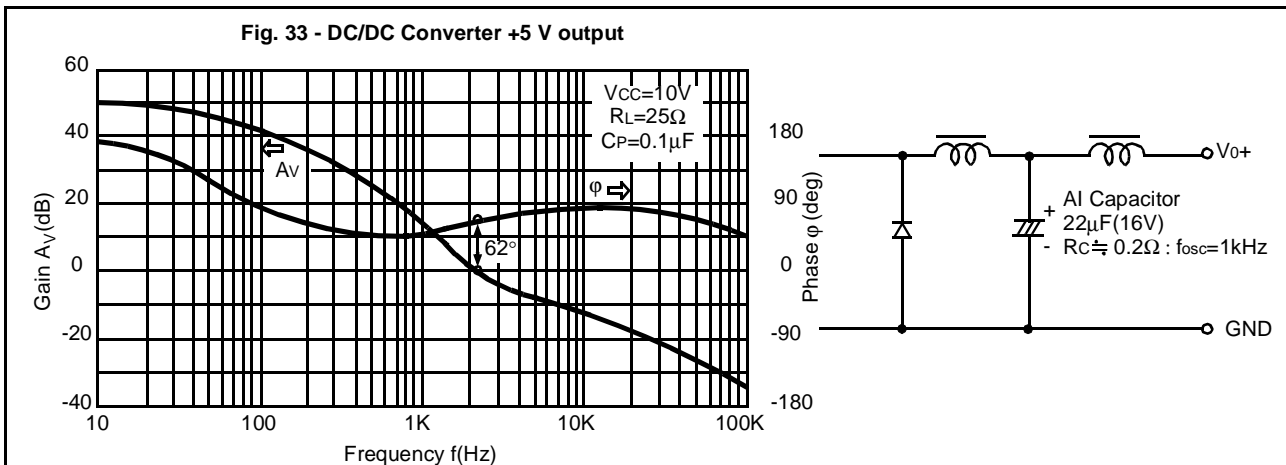
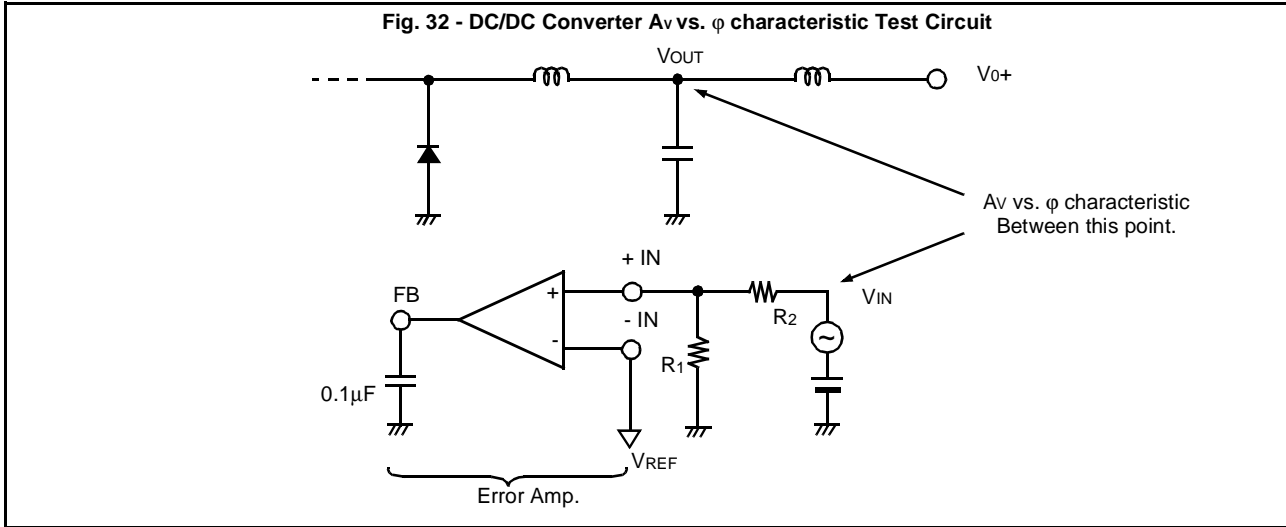


Fig. 31 - Phase vs. Frequency



Reference data

If an aluminum electrolytic smoothing capacitor ($R_c \approx 1.0\Omega$) is replaced with a low ESR semiconductor electrolytic capacitor (OS-CON: $R_c \approx 0.2\Omega$), the phase shift is reduced by half (see Fig. 33 and 34).



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3. Measures for ensuring system stability when a low ESR smoothing capacitor is used

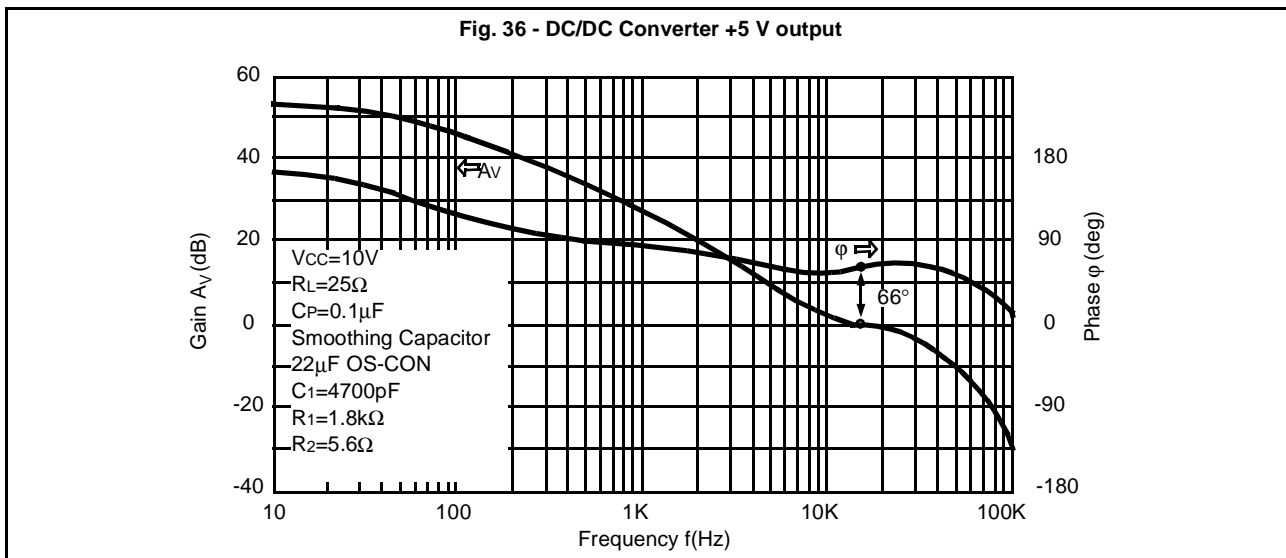
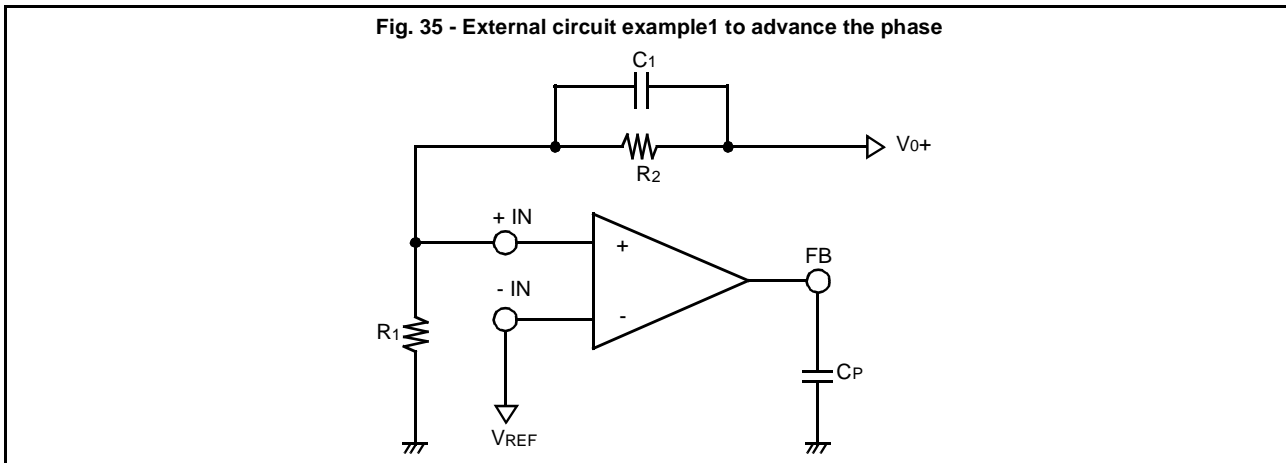
When a low ESR smoothing capacitor is used in the DC/DC converter, only the L and C are apparent even in the high-frequency region, and the phase is delayed by almost 180°. Consequently, the system phase margin and stability are reduced. On the other hand, a low ESR capacitor is needed to reduce the amount of output ripple. This is contrary to the system stability explained above. To solve this problem, phase compensation can be used. This method increases the phase margin by advancing the phase when the phase margin is reduced by a low ESR capacitor.

The three suggestions listed below are recommended for DC/DC converters using the MB3775.

- (1) As shown in Fig. 35, a capacitor is connected in parallel with the output feedback resistor to advance the phase. Use the formula below as a guideline for the capacitance.

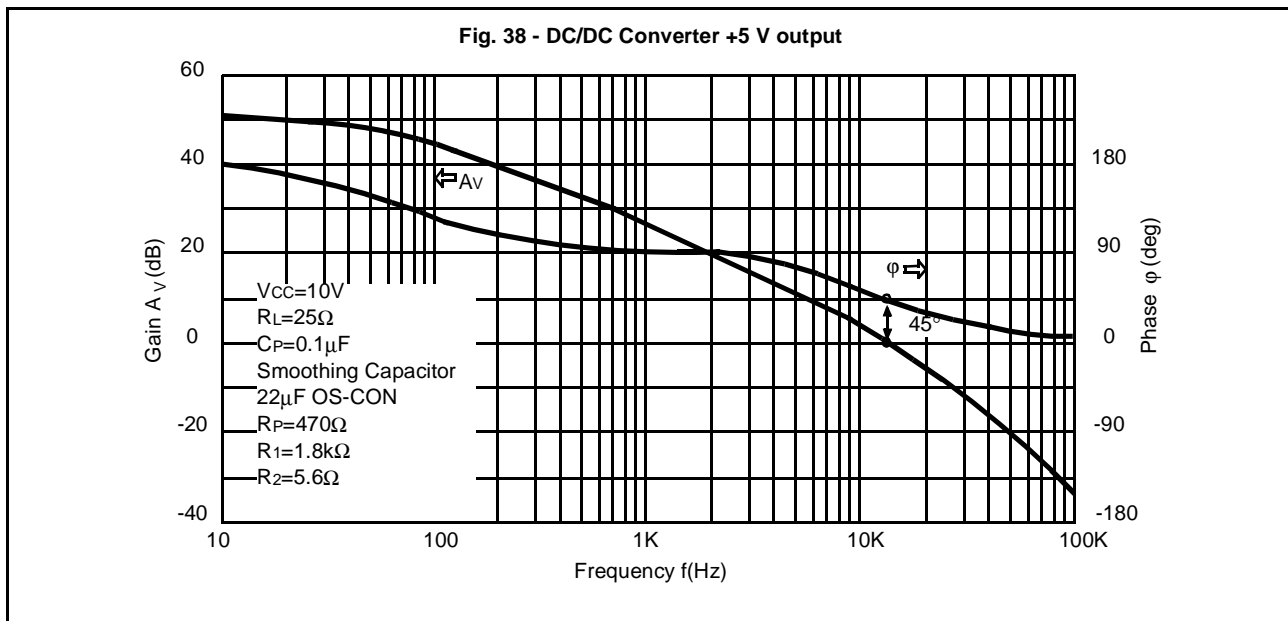
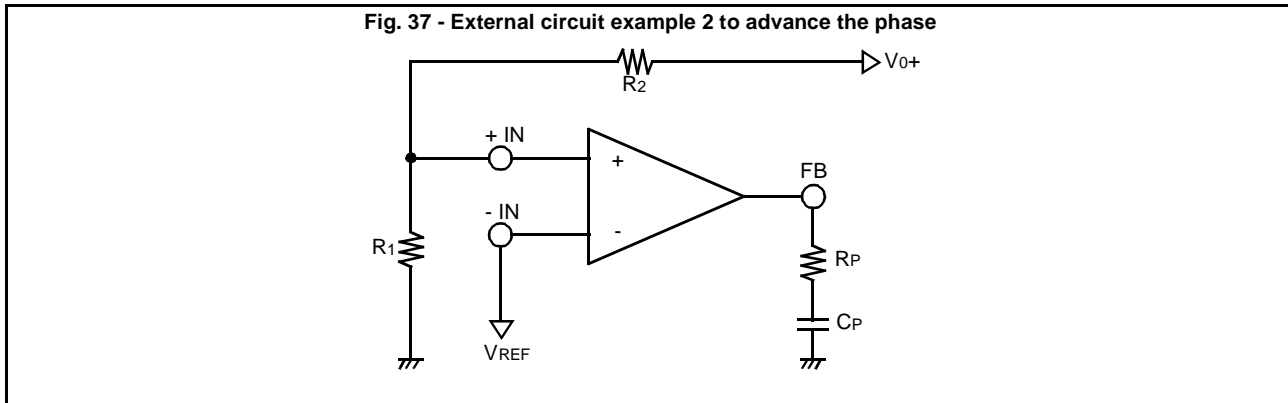
$$C1 \approx \frac{1}{2\pi f R2}$$

↑ Unstable Frequency (See Fig. 32)



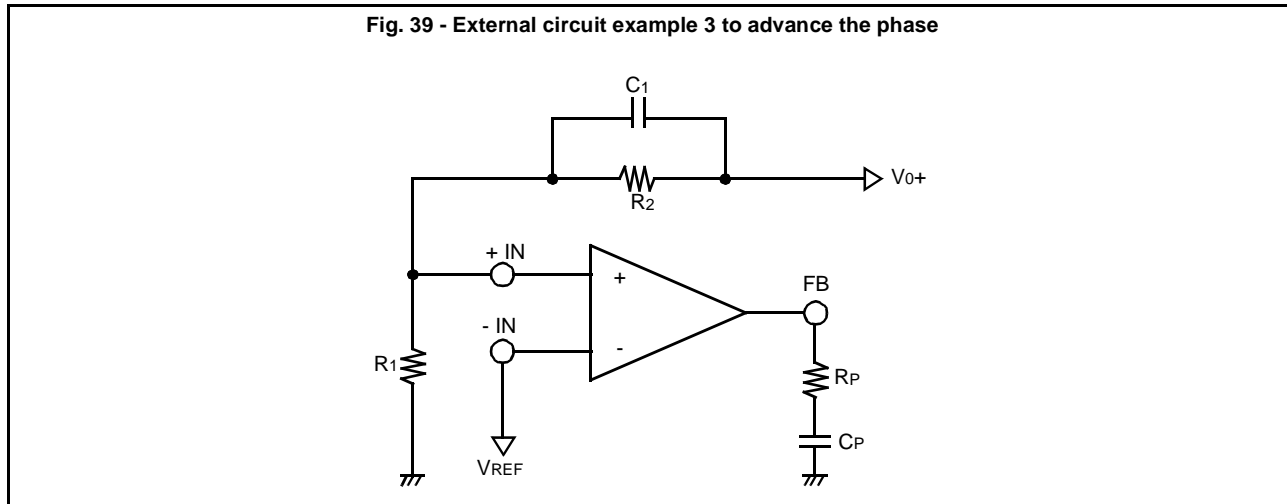
3. Measures for ensuring system stability when a low ESR smoothing capacitor is used (Continued)

(2) As shown in Figure 37, a resistor (R_P) is connected between the FB terminal and C_P of the error amplifier to advance the phase. The more R_P is increased, the more the phase is advanced. However, the gain in the high-frequency range is also increased, which causes instability. Therefore, select the optimum resistance (see Fig. 38).



MB3775

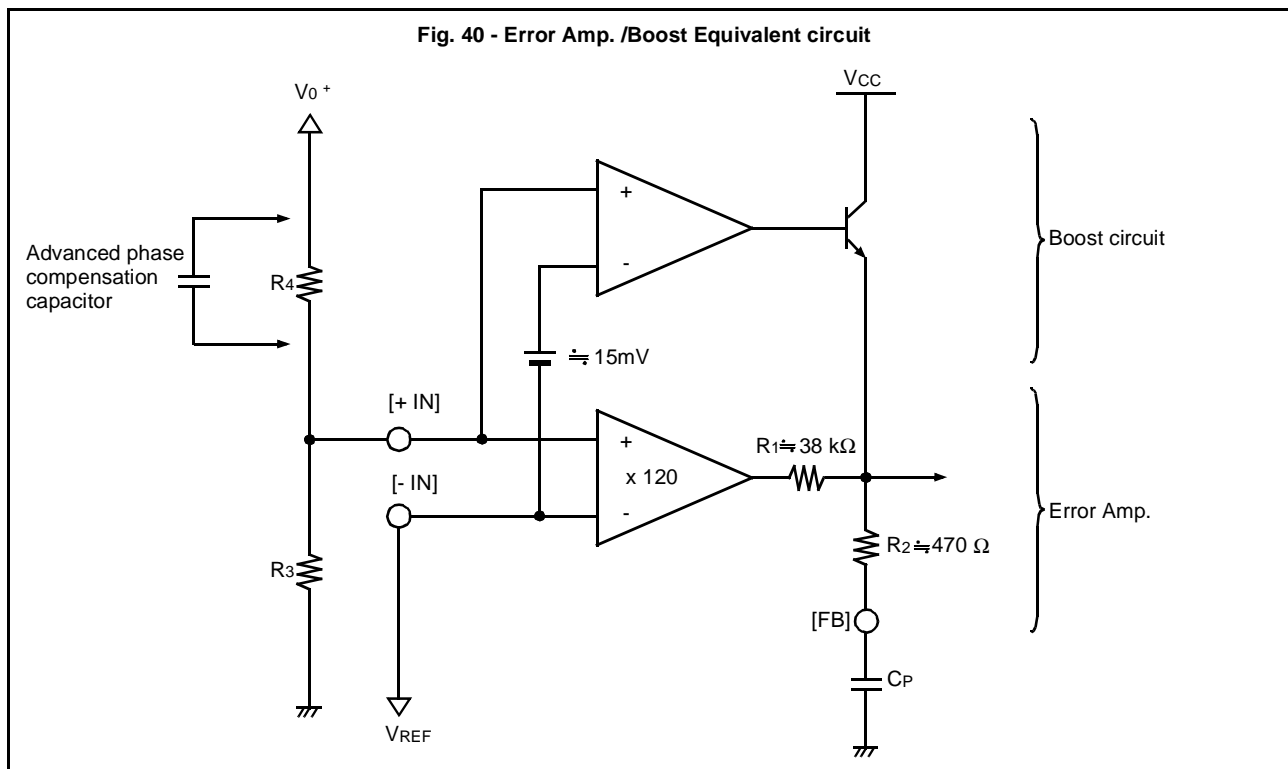
(3) As shown in Fig. 39, the phase is advanced by using both example 1 and 2 (Fig. 35 and 37).



4. Error amplifier input ripple voltage

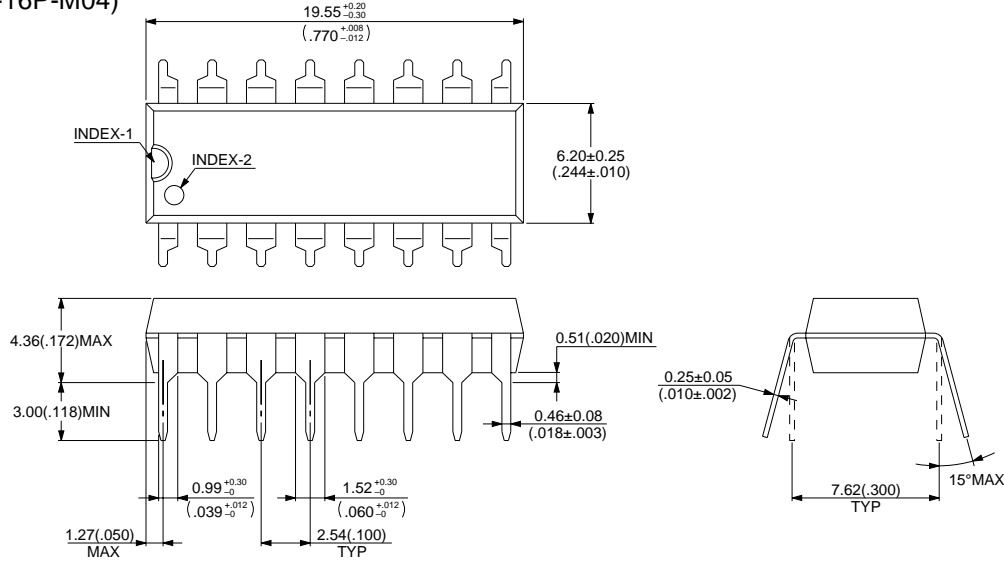
The boost circuit for charging the phase compensating capacitor C_P is connected to the error amplifier as shown in Figure 40 to protect against output voltage overload at power-on.

A 15 mV offset voltage is provided for the negative input side so that the boost circuit only operates at power-on. When a capacitor is connected in parallel with the output feedback resistor, because the output ripple is too large or for advanced phase compensation, the boost circuit starts operating, which may degrade regulation if the differential input voltage of the error amplifier exceeds 15 mV. Be careful with the differential input voltage of the error amplifier.



■ PACKAGE DIMENSIONS

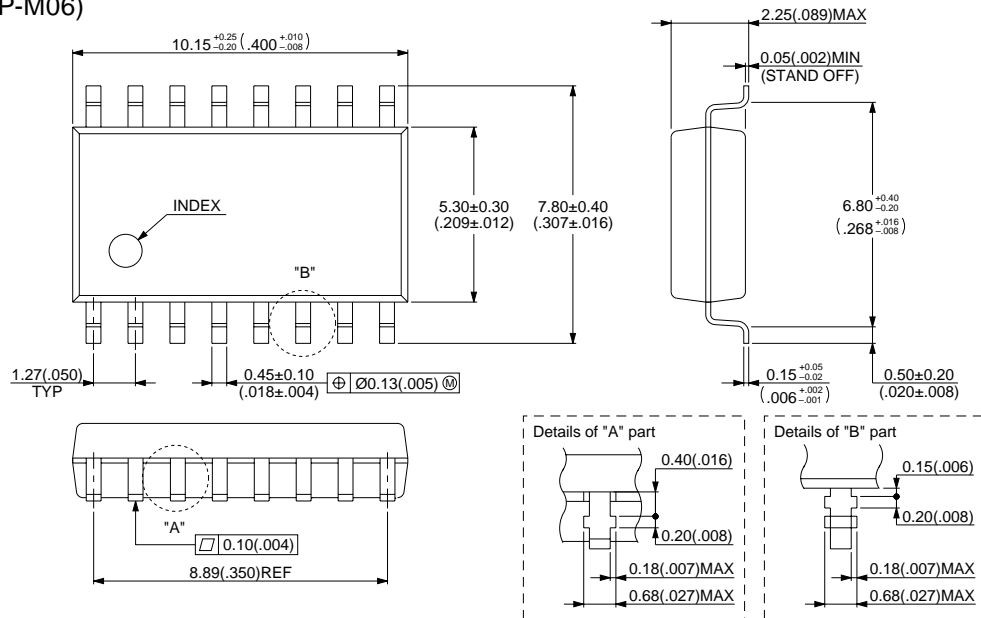
16 pins, Plastic DIP
(DIP-16P-M04)



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Dimensions in mm (inches).

16 pins, Plastic SOP
(FPT-16P-M06)

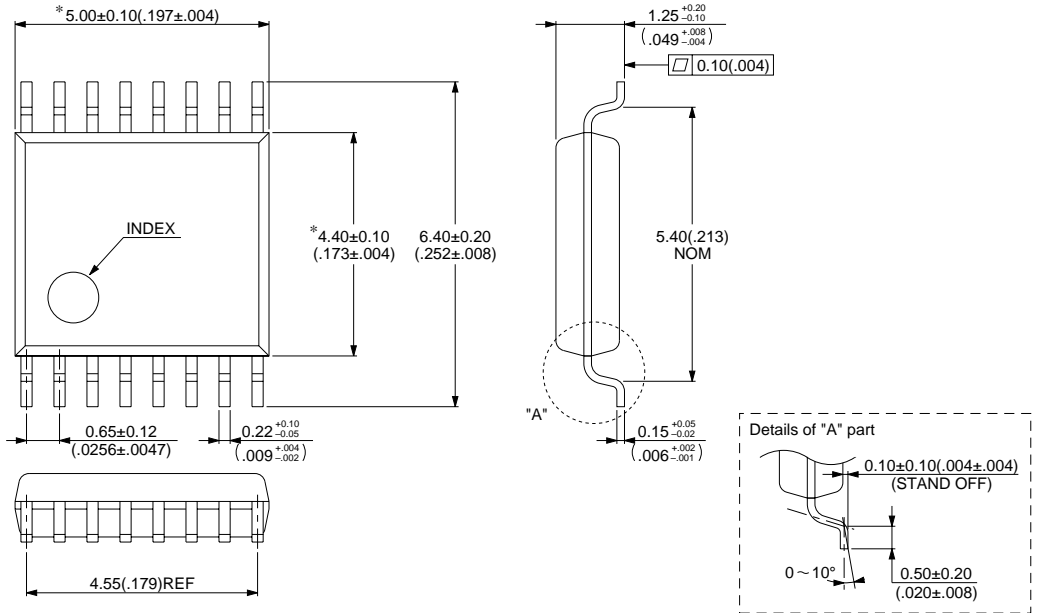


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Dimensions in mm (inches).

MB3775

16 pins, Plastic SOP
(FPT-16P-M05)



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Dimensions in mm (inches).

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